

**REMARKS**

**35 USC §112**

Claims 8-12 and 29-33 are rejected under 35 USC §112 as failing to comply with the written description requirement. The Applicant respectfully disagrees. Claims 8 and 29 are herein amended as part of another section of this response, and through those amendments, the rejection has been mooted.

**35 USC 103 (A)**

Claims 1-6, 8-15, 17-27 and 29-38 were rejected under 35 USC §103(a) as being unpatentable over the admitted prior art in view of Hussein et al (US 6,037,255), Avanzino et al. (US 5,795,823) and Pellerin et al. The Applicant respectfully disagrees.

Claim 1 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer, an etchstop layer applied to the first organic intermetal dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide; b) forming a via opening in said stack; c) depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a line opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer, an etchstop layer applied to the first organic intermetal

dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and substantially covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material.

The Applicant has reviewed the three cited references in detail, and none of the references, alone or in combination teach, motivate or suggest to one of ordinary skill in the art to form a stack with a first organic intermetal dielectric layer, an etchstop layer applied to the first organic intermetal dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide. In the present application, three dielectric layers are taught – two organic intermetal dielectrics and one sacrificial inorganic dielectric layer.

For example, Pellerin in the Background Section (Column 1, lines 35-51) teaches that the technique of having one layer of dielectric material, an etch stop layer and another layer of dielectric material is known and is also not needed in the teachings of his invention. Pellerin states that an etch stop layer and a hard mask layer is not needed, because of the organic intermetal dielectric layer coupled to the sacrificial inorganic dielectric layer.

Avanzino (as the Examiner points out) mentions having two dielectric layers whereby the layers are split with an etch stop layer. However, Avanzino does not teach a third dielectric layer (whether sacrificial or not) in addition to the two previously mentioned. There cannot be any combination of Avanzino and Pellerin either, because Pellerin teaches away from using an etch stop layer and a hard mask layer. Furthermore, the Examiner uses Avanzino solely as the reason for rejecting previously submitted claims 8 and 29 for the reason that there are two layers separated by an etch stop, but there is nothing in Avanzino to suggest two layers separated by an etch stop coupled

with a hard mask and a sacrificial inorganic dielectric layer. And, as mentioned, the Applicant cannot possibly see the combination of Avanzino with either Pellerin (who teaches against an etchstop) and Hussein (who does not have three effective dielectric layers applied before the conductive layer is applied).

**REQUEST FOR ALLOWANCE**

Claims 1-6, 8-15, 17-27 and 29-38 are pending in this application, and the Applicant respectfully requests that the Examiner reconsider all of the claims in light of the arguments presented and allow all current and pending claims.

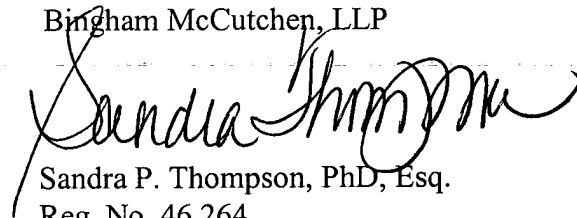
The Applicant also respectfully requests that the Examiner contact the undersigned Attorney-of-Record for a teleconference, if all patentability issues aren't resolved in the Applicant's favor, so that they can all be resolved as quickly as possible.

Respectfully submitted,

Bingham McCutchen, LLP

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Please acknowledge receipt of the following by affixing hereon the Official date stamp and returning this card to our office.

**Title:** Request for Continued Examination  
Use of Sacrificial Inorganic Dielectrics for Dual Damascene Processes. . .  
**Inventor:** Honeywell (WFM) - Joseph Kennedy, et al.  
**Filing Date:** 11 April 2000  
**Serial Number:** 09/547167  
**Matter Type:** Patent - US  
**Date of Deposit:** November 18, 2003  
**Matter #:** 7210522001-3221000  
**Enclosures:** (1) RCE Transmittal (3 pages); (2) Preliminary Amendment (11 pages); and (3) postcard.

DATE MAILED: 11/18/03 SBU: 4780  
PATENT APPLICATION FOR: Use of Sacrificial Inorganic...

INVENTOR(S): Kennedy, et al.  
SERIAL NO.: 09/547,167

**THE FOLLOWING HAS BEEN RECEIVED IN THE U.S. PATENT AND TRADEMARK OFFICE ON THE DATE STAMPED HEREON:**

☐ Missing Parts of Application Transmittal \$ \_\_\_\_\_  
☐ Combined Declaration/Power of Attorney \$ \_\_\_\_\_  
☐ Power of Attorney  
☐ Assignment and Cover Sheet: \$ \_\_\_\_\_  
☐ Information Disclosure Statement ☐ ISR ☐ From PTO 1449 with \_\_\_\_\_ References \$ \_\_\_\_\_  
☐ Request for Corrected Filing Receipt  
☐ Amendment/Response ( \_\_\_\_\_ page(s)) \$ \_\_\_\_\_  
☐ Petition for Extension of Time ( \_\_\_\_\_ months) \$ \_\_\_\_\_  
☐ Amendment After Final Rejection ( \_\_\_\_\_ page(s)) \$ \_\_\_\_\_  
☐ Notice of Appeal  
☐ Appeal Brief ( \_\_\_\_\_ page(s)) \$ \_\_\_\_\_  
☐ Issue Fee Transmittal \$ \_\_\_\_\_  
☐ Formal Drawing(s); No. of Sheets \_\_\_\_\_  
☐ Total fees charged to Deposit Account No. 01-1125: \$ \_\_\_\_\_  
OTHER PCC \$ 770.  
Attorney Docket No.: 304885 Attorney: Krschmer  
Outside Counsel: Bingham

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